

What is claimed is:

1. A semiconductor integrated circuit device comprising a plurality of vertical MISFETs,

wherein the vertical MISFET comprises

(a1) a columnar laminate having, at the upper portion and lower portion thereof, a first and second semiconductor regions, respectively, and

(a2) a conductive film formed over the side walls of the columnar laminate via a first insulating film,

wherein the plurality of vertical MISFETs having the columnar laminate and the conductive film are

(b1) spaced by a first distance in a first direction, and

(b2) spaced by a second distance, which is greater than the first distance, in a second direction, and

wherein up to at least a predetermined height of the columnar laminate of the plurality of vertical MISFETs,

(c1) a second insulating film is formed in a space between the columnar laminates in the first direction, and

(c2) the second insulating film and a third insulating film lying thereover are formed in a space between the columnar laminates in the second direction.

2. A semiconductor integrated circuit device, comprising:

a plurality of vertical MISFETs each including,

(a1) a columnar laminate having, at the upper portion and lower portion thereof, first and second semiconductor regions respectively, and

(a2) a conductive film formed over the side walls of the columnar laminate via a first insulating film,

wherein said vertical MISFETs is arranged in an array form, such that

(b1) the vertical MISFETs are spaced by a first distance in a first direction, and such that

(b2) vertical MISFETs are spaced by a second distance, which is greater than the first distance, in a second direction;

(c) a second insulating film having, embedded therein, the vertical MISFETs aligned in the first direction, out of the plurality of vertical MISFETs, and having a plurality of projecting portions extending in the first direction; and

(d) a third insulating film formed between the plurality of projecting portions of the second insulating film.

3. A semiconductor integrated circuit device according to claim 1, wherein the second insulating film has better coverage than the third insulating film.

4. A semiconductor integrated circuit device according to claim 1, wherein the second insulating film is

a silicon oxide film formed by chemical vapor deposition by using tetraethoxysilane as a raw material, and

the third insulating film is a silicon oxide film formed under a plasma atmosphere having a plasma density of  $10^{11}/\text{cm}^2$  or greater.

5. A semiconductor integrated circuit device according to claim 4, wherein the second insulating film is a silicon oxide film formed by chemical vapor deposition by using tetraethoxysilane and ozone ( $\text{O}_3$ ) as raw materials.

6. A semiconductor integrated circuit device according to claim 1, wherein the columnar laminate has a high at least 3 times as much as that of the first distance.

7. A semiconductor integrated circuit device according to claim 1, wherein the first distance is 150 nm or less, while the second distance is 500 nm or greater.

8. A semiconductor integrated circuit device according to claim 1, wherein a fourth insulating film is filled in spaces, in the first direction and in the second direction, between the columnar laminates on and above a predetermined height thereof.

9. A semiconductor integrated circuit device according to claim 1, wherein a thickness of the second insulating film in the space between the columnar laminates in the second direction is the first distance or greater.

10. A semiconductor integrated circuit device

according to claim 1, wherein the plane pattern of the columnar laminate and the conductive film over the side walls thereof is approximately elliptical and a first diameter in the first direction is smaller than a second diameter in the second direction.

11. A semiconductor integrated circuit device according to claim 1, wherein the predetermined height exists between the bottom and top of the first semiconductor region.

12. A semiconductor integrated circuit device according to claim 1, wherein the plurality of vertical MISFETs constitute a plurality of memory cells disposed in the array form in the first and second directions,

the memory cells each including:

(d1) of the plurality of vertical MISFETs, two vertical MISFETs adjacent in the first direction;

(d2) two horizontal drive MISFETs connected to the respective second semiconductor regions of the two vertical MISFETs, respectively, and together with the two vertical MISFETs, constituting a pair of inverters having input and output portions cross-connected; and

(d3) two horizontal transfer MISFETs each connected between the second semiconductor region of each of the two vertical MISFETs and a first line pair and having a gate electrode connected to a second line,

(d4) wherein the two horizontal drive MISFETs and two horizontal transfer MISFETs are formed below the second semiconductor region.

13. A semiconductor integrated circuit device according to claim 1, wherein the plurality of vertical MISFETs constitute a plurality of memory cells disposed in the array form in the first and second directions,

the memory cells each including:

(d1) of the plurality of vertical MISFETs, two vertical MISFETs which are adjacent in the first direction, in which each has the second semiconductor region connected to a first line pair, and

each has the conductive film connected to a second line;

(d2) two horizontal drive MISFETs connected between each of the second semiconductor regions of the two vertical MISFETs and a reference potential, and having a gate electrode cross-connected to each of the second semiconductor regions of the two vertical MISFETs,

(d3) wherein the two horizontal drive MISFETs are formed below the second semiconductor region.

14. A semiconductor integrated circuit device according to claim 12, wherein a single region in which the memory cell is formed is approximately rectangular and the length thereof is greater in the second direction than that

in the first direction.

15. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of columnar laminates having, at the upper portion and lower portions thereof, a first semiconductor region and a second semiconductor region, respectively, while spacing the plurality of columnar laminates in a first direction and in a second direction wider than the first direction;

(b) forming conductive films over the side walls of the columnar laminates via a first insulating film with a distance, in the first direction, between the conductive films over the side walls of the plurality of columnar laminates as a first distance and with a distance in the second direction as a second distance which is greater than the first distance;

(c) forming a second insulating film to a thickness enough to fill a space of the first distance and but not enough to fill a space of the second distance; and

(d) forming a third insulating film over the second insulating film and filling the space of the second distance.

16. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of columnar laminates having,

at the upper portion and lower portions thereof, a first semiconductor region and a second semiconductor region, respectively, while spacing the plurality of columnar laminates in a first direction and in a second direction wider than the first direction;

(b) forming conductive films over the side walls of the columnar laminates via a first insulating film with a distance, in the first direction, between the conductive films over the side walls of the plurality of columnar laminates as a first distance and with a distance in the second direction as a second distance which is greater than the first distance;

(c) depositing a second insulating film between the columnar laminates and thereover with a thickness at least equal to the first distance; and

(d) depositing over the second insulating film a third insulating film with a thickness corresponding to at least 70% of a vertical difference, after the step (c), between the top of the second insulating film over the second distance portion of the columnar laminates and the top of the second insulating film over the columnar laminates.

17. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the step (c) is carried out at a temperature of 700°C or

less.

18. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the step (c) and the step (d) are carried out at a temperature of 700°C or less.

19. A manufacturing method of a semiconductor integrated circuit device according to claim 15, further comprising, after the step (d), the steps of:

(e) depositing a fourth insulating film over the third insulating film; and

(f) etching the second, third and fourth insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is exposed.

20. A manufacturing method of a semiconductor integrated circuit device according to claim 19, further comprising, after the step (g), a steps of:

(h) forming a fifth insulating film over the second and third insulating films.

21. A manufacturing method of a semiconductor integrated circuit device according to claim 15, further comprising, after the step (d), the steps of:

(e) etching the second and third insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is

exposed; and

(f) etching the conductive film exposed by the step (e).

22. A manufacturing method of a semiconductor integrated circuit device according to claim 21, further comprising, after the step (f), a step of:

(g) forming a fourth insulating film over the second and third insulating films.

23. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the second insulating film has better coverage than the third insulating film.

24. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the second insulating film is a silicon oxide film and the step (c) is carried out by chemical vapor deposition using tetraethoxysilane as a raw material.

25. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the second insulating film is a silicon oxide film and the step (c) is carried out by chemical vapor deposition using tetraethoxysilane and ozone ( $O_3$ ) as raw materials.

26. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the third insulating film is a silicon oxide film and the

step (d) is carried out in a plasma atmosphere having a plasma density of  $10^{11}/\text{cm}^2$  or greater.

27. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the columnar laminate has a height of at least 3 times as much as the first distance.

28. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the first distance is 150 nm or less and the second distance is 500 nm or greater.

29. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the plane pattern of each of the columnar laminate and the conductive film over the side walls thereof is approximately elliptical and a first diameter in the first direction is smaller than a second diameter in the second direction.

30. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the columnar laminate in the step (a) is formed using a mask which is H-shaped in the first direction.

31. A manufacturing method of a semiconductor integrated circuit device according to claim 15, further comprising, prior to the step (a), the steps of:

(h) forming two pairs of horizontal MISFETs having

source and drain regions in common; and

(i) connecting the second semiconductor regions of the two vertical MISFETs adjacent to each other in the first direction to the source and drain regions which the two pairs of horizontal MISFETs have in common, respectively.

32. A manufacturing method of a semiconductor integrated circuit device according to claim 15, further comprising, prior to the step (a), the steps of:

(j) forming two horizontal MISFETs; and

(k) connecting the second semiconductor regions of the two vertical MISFETs adjacent to each other in the first direction to one ends of the two horizontal MISFETs, respectively.

33. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a semiconductor film having, at the upper and lower portions thereof, first and second semiconductor regions, respectively;

(b) etching the semiconductor film through a mask which is H-shaped in first direction, thereby forming an approximately elliptical columnar laminate having a longer diameter in a second direction perpendicular to the first direction; and

(c) forming a conductive film over the side walls of

the approximately elliptical columnar laminate via an insulating film.

34. A manufacturing method of a semiconductor integrated circuit device comprising a plurality of vertical MISFETs,

wherein the vertical MISFET comprises

(a1) a columnar laminate having, at the upper and lower portions thereof, first and second semiconductor regions, respectively, and

(a2) a conductive film formed over the side walls of the columnar laminate via a first insulating film,

wherein said plurality of vertical MISFETs having the columnar laminate and conductive film are

(b1) spaced by a first distance in a first direction, and

(b2) spaced by a second distance, which is greater than the first distance, in a second direction,

(c) the plane pattern of the columnar laminate and the conductive film over the side walls thereof being approximately elliptical, and a first diameter in the first direction being smaller than a second diameter in the second direction,

the method comprising the steps of:

(d) forming a semiconductor film, having at the upper and lower portions thereof, first and second semiconductor

regions, respectively; and

(e) etching the semiconductor film via a mask which is H-shaped in the first direction, thereby forming an approximately elliptical columnar laminate having a longer diameter in a second direction perpendicular to the first direction.

35. A manufacturing method of a semiconductor integrated circuit device according to claim 33, wherein the steps are for the formation of vertical MISFETs constituting a SRAM, and a single memory cell formation region of the SRAM is approximately rectangular with a long side in the second direction.

36. A semiconductor integrated circuit device according to claim 33, wherein the H-shaped mask is a transfer mask used in photolithography, an approximately elliptical columnar pattern for etching is formed using the H-shaped transfer mask, and the semiconductor film is processed into an approximately elliptical columnar laminate by using the etching pattern.

37. A semiconductor integrated circuit device according to claim 36, wherein the H-shaped mask has a structure in which the width of the mask in the first direction is narrower at the center of the mask in the second direction than at the both ends.

38. A semiconductor integrated circuit device,

comprising:

(a) a columnar laminate having, at the upper and lower portions thereof, first and second semiconductor regions, respectively and having an approximately elliptical plane pattern; and

(b) a conductive film formed over the side walls of the columnar laminate via an insulating film.

39. A semiconductor integrated circuit device comprising a plurality of vertical MISFETs including:

(a1) a columnar laminate having, at the upper portion and lower portion thereof, first and second semiconductor regions, respectively; and

(a2) a conductive film formed over side walls of the columnar laminate via a first insulating film,

wherein the plurality of vertical MISFETs having the columnar laminate and the conductive film are

(b1) spaced by a first distance in a first direction, and

(b2) spaced by a second distance, which is greater than the first distance, in a second direction, and

(c) wherein a plane pattern of the columnar laminate and the conductive film over the side walls thereof is approximately elliptical and a first diameter in the first direction is smaller than a second diameter in the second direction.

40. A semiconductor integrated circuit device according to claim 38, wherein the columnar laminate constitutes the vertical MISFET of SRAM, and a single memory cell formation region of the SRAM is approximately rectangular and has a long side in the direction of a longer diameter of the approximately elliptical shape.

41. A semiconductor integrated circuit device according to claim 1, wherein the conductive film is formed to encompass the columnar laminate.

42. A manufacturing method of a semiconductor integrated circuit device according to claim 15, wherein the conductive film is formed to encompass the columnar laminate.